Remarks

Below, the applicant's comments are preceded by related remarks of the examiner set forth in small bold font.

> **Claims 13, 16, 24, 26 and 27 are rejected under 35 U.S.C. 102(e) as being clearly anticipated by Clarke US 6,337,604 (Clarke).**
>
> **The single Figure of Clarke discloses a circuitry for controlling the oscillating frequency of an oscillator (See column 2, line 22), the circuitry having a plurality of on-chip capacitors C 1 -C6, each of which is independently selectable by a control signal D0-D5, and each of which provides a controllable amount of capacitance to the oscillator to control the oscillating frequency of the oscillator (See column 2, line 22).**
>
> **The single Figure of Clarke also discloses an electronic device comprising a real time clock, i.e. oscillator, for generating a system time signal "CLK OUT 5" (See the only Figure and column 2, around line 20), the real time clock having a digitally tunable oscillator (Note the use of set of shift registers 21) for digitally adjusting an operating frequency of the real time clock to speed up or slow down the system time signal (See column 3, lines 49, and a memory device 21 for storing data representing a configuration of the digitally adjusted tunable oscillator.**
>
> ...
>
> **Claims 14, 17 and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Clarke and Ochiai as applied to claims 1-6, and 30-35 above, and further in view of Theus et al. US 5,805,029 (Theus).**
>
> ...
>
> **Claims 15, 28, and 29 are rejected under 35 U.S.C. 103(a)as being unpatentable over Clarke US 6,337,604 (Clarke).**

As discussed in the telephone interview with the Examiner on November 18, 2003, Clarke does not disclose or suggest "a circuit to generate a system time signal based on the real time clock signal, the system time signal representing at least one of hour, minute, and second," as recited in amended claim 13.

Clarke merely discloses a "standard CMOS clock signal (clk-out)" (col. 2, lines 20-21) whose frequency can be adjusted. The "clock signal" in Clarke does not represent at least one of hour, minute, and second.

Claims 14, 15, and 28 are patentable for at least the same reasons as claim 13.

> **As it relates to at least claim 16, Clarke also discloses a method for generating a set of control signals Do-D5 to select a subset of capacitors from a set of capacitors C1-C6, connecting the selected subset**

of capacitors to an oscillator 1, generating an oscillating signal using the oscillator and the selected subset of capacitors in combination, and generating a system time signal CLK OUT 5 (See the only Figure in Clarke) using the oscillating signal.

...

Claims 14, 17 and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Clarke and Ochiai as applied to claims 1-6, and 30-35 above, and further in view of Theus et al. US 5,805,029 (Theus).

Clarke does not disclose or suggest "generating a system time signal using the oscillating signal, the system time signal representing at least one of hour, minute, and second," as recited in amended claim 16.

Claims 17 and 18 are patentable for at least the same reasons as claim 16.

As it relates to at least claim 24 the only figure of Clarke clearly illustrates an apparatus having a control unit 7, 23, 21 configured to generate a set of control signals Do-D5, each of which independently selects a capacitor from a plurality of capacitors, the selected capacitors being coupled to an oscillator 1, the selected capacitors in combination proving a controllable amount of capacitance to the oscillator to control the oscillating frequency of the oscillator (See column 2, line 22). As it clearly apparent from the only Figure of Clarke the system time signal CLK OUT 5 shown in the only Figure is based upon the oscillating frequency of the oscillator. The data processing unit 23 processes the data based on the system time signal that is applied to the element 7 of Clarke and the register stores the configuration of the set of control signals as are both clearly apparent from the only Figure in Clarke.

...

Claim 25 is rejected under 35 USC 103 as being obvious over Horn "Basic Electronics Theory " pp 418-426 (Horn) in view of Clarke US 6,337,604 (Clarke).

Clarke does not disclose or suggest "circuitry to generate a system time signal representing at least one of hour, minute, and second based on the real time clock signal," as recited in amended claim 24.

Claims 25, 27, and 29 are patentable for at least the same reasons as claim 24.

Claims 1-6, and 30-35 are rejected under 35 U.S.C. 103(a) as being unpatentable over Clarke US 6,337,604 (Clarke)in view of Ochiai et al. US 4,851,792 (Ochiai).

All the same reasoning as applied in the 35 USC 102 rejection of claims 13, 16,24, 26 and 27 and the following: Claim 1 has been

amended to recite a bias circuit to provide a substantially constant voltage to the bias at least one of the plurality of capacitors. Claim 35 recites the formation of a time signal that is clearly present in Clarke as noted above.

Claims 3-6 and 33 recite conventional forms of capacitors that make up the frequency changing capacitors of the oscillator. Clarke is silent on these.

Accordingly, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have substituted any of the conventional capacitors as recited by the claims of the instant application in place of the generic capacitors of Clarke because, as the reference is silent as to the exact composition of the capacitors, any art-recognized equivalent capacitors would have been usable such as the well-known capacitors as recited by the claims of the instant application.

As it relates to claim 2, selection of the frequency changing capacitors to be different from each other is merely the selection of the optimum or workable range. This involves but routine skill in the art and accordingly it would have been obvious to one of ordinary skill in the art at the time the invention was made to select the capacitance values to be any value within the optimum or workable range so as to shift the frequency in a controllable predetermined stepwise manner.

As it relates to newly amended claim 1, Figure 8(a) discloses a biasing arrangement for the capacitors of an oscillator and is configured such that the bias voltage VB of the capacitor 14 "remains constant". This as recognized by Ochiai allows for the oscillation frequency to remain constant (See column 5, around line 61).

Thus it would have been obvious to one of ordinary skill in the art at the time the invention was made to provide the oscillator arrangement of Clarke with a bias arrangement that keeps the necessary bias voltage of the capacitor elements constant so as to prevent drift in oscillator frequency as taught by Ochiai.

...

Claims 7 and 8 are rejected under 35 U.S.C. 103(a)as being unpatentable over Clarke and Ochiai as applied to claims 1-6, and 30-35 above, and further in view of Kuhn Jr. US 3,930,169 (Kuhn, Jr.).

...

Claims 9 and 10 are rejected under 35 U.S.C. 103(a)as being unpatentable over Clarke, Ochiai and Kuhn, Jr. as applied to claims 1-8, and 30-35 above, and further in view of Horn "Basic Electronics Theory" 4th Edition pp 377-378 and pp 454-465.

...

Claims 11 and 12 are rejected under 135 U.S.C. 103(a)as being unpatentable over Clarke and Ochiai as applied to claims 1-6, and 30-35 above, and further in view of Leduc et al. US 6,400,231 (Leduc)

Regarding claim 1, there is no motivation to combine Clarke and Ochiai. Clarke does not disclose or suggest any bias circuit to bias a capacitor, and there is no suggestion that the

capacitors need any bias voltage to operate. Clarke discloses an oscillator circuit whose output frequency can be varied by adjusting the amount of capacitance coupled to a crystal (1). The amount of capacitance is adjusted by selecting different combinations of capacitors C1-C6. Ochiai discloses a bias circuit for biasing a floating gate MOS variable capacitor (14), whose capacitance can be varied by injecting electrons into a floating gate (see FIG. 8(a) and col. 2, line 65 to col. 3, line 5). There is no incentive to use the floating gate MOS variable capacitor of Ochiai in the oscillator circuit of Clarke, and therefore, there is no motivation to use the bias circuit of Ochiai in the oscillator circuit of Clarke.

Because Ochiai uses a floating gate MOS variable capacitor whose capacitance can be varied, there is no motivation to use the capacitor bank of Clarke in the oscillator circuit of Ochiai.

For the above reasons, claim 1 would not have been obvious in view of Clarke and Ochiai. The feature of claim 1 lacking in Clarke and Ochiai is also not disclosed or suggested by Kuhn, Horn, or Leduc.

Claims 2-12 and 30-32 are patentable for at least the same reasons as claim 1.

Regarding claim 33, it is not true that all conventional capacitors are suitable for use in an oscillator circuit. For example, a drain-source connected P-type MOSFET may not operate properly if the biasing circuit shown in FIG. 2 (including R_{bias} and C_{bias}) were not used. Many common configurations of connecting a MOSFET capacitor may not be suitable for use in an oscillator circuit and may cause problems, such as having a capacitance that varies with the oscillating signal, having noise coupled from the power supply to cause glitches in the output signal, or having leakage current that affects the DC bias level of other parts of the oscillator circuit.

It was the applicant who first conceived the idea of using drain-source connected MOSFETs in an oscillating circuit. In one example, enhancement mode P-type MOSFETs are used, with the gate nodes coupled to the oscillating signal and the drain-source nodes connected to a bias circuit, which provides a substantially constant bias voltage and filters out noise from the power supply. In another example, depletion mode N-type MOSFET devices are used, with

the gate nodes coupled to the oscillating signal and the drain-source nodes connected to the ground reference.

The applicant respectfully requests the examiner to provide a reference that suggests drain-source connected MOSFET capacitors can be used as load capacitors of an oscillator circuit.

The discussion above relating to criteria for configuring MOSFET capacitors merely shows that it would not have been obvious to use a drain-source connected MOSFET capacitor in an oscillator circuit. The discussion is not intended to limit the claim scope in any way.

Claims 34 and 35 are patentable for at least the same reasons as claim 33.

Please apply any charges or credits to deposit account 06-1050, referencing attorney docket 10559-650001.

Respectfully submitted,

Date: December 8, 2003

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* See attached document certifying that Rex Huang has limited recognition to practice before the U.S. Patent and Trademark Office under 37 CFR § 10.9(b).

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Expires: May 16, 2004

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